WHAT IS CLAIMED IS:

1. An A/D conversion method for a serial/parallel A/D converter which compares an analog input voltage which randomly varies with time and a prescribed first reference voltage, to generate a first binary code, as well as compares a second reference voltage which is decided on the basis of the result of the comparison and the analog input voltage, to generate a second binary code, and performs a logic operation on the generated first and second binary codes, thereby generating a digital value, said method comprising:

a sampling and initialization step of sampling the analog input voltage received, as well as initializing a previous second reference voltage to a prescribed initialization voltage;

a first voltage comparison step of comparing the value of the analog input voltage which has been sampled in the sampling and initialization step and the first reference voltage, to generate the first binary code; and

a second voltage comparison step of comparing the value of the second reference voltage which has been changed from the prescribed initialization voltage to a voltage which is decided on the basis of the result of the comparison in the first voltage comparison step, with the value of the analog input voltage which has been sampled in the sampling and initialization step, to generate the second binary code.

2. An A/D conversion method for a serial/parallel A/D converter which compares an analog input voltage which randomly varies with time and a prescribed first reference voltage, to generates a first binary code, as well as compares a second reference voltage which is decided on the basis of the result of the comparison, and the analog input voltage, to generates a second binary code, and performs a logic operation on the generated first and second binary codes, thereby generating a digital value, said method comprising:

a sampling step of the sampling analog input voltage received;

a first voltage comparison and initialization step of comparing the analog input voltage which has been sampled in the sampling step and the first reference voltage, and initializing a previous second reference voltage to a prescribed initialization voltage, to generate the first binary code; and

a second voltage comparison step of comparing the second reference voltage which has been changed from the prescribed initialization voltage to a voltage value which is decided on the basis of the result of the comparison in the first voltage comparison and initialization step, and the analog input voltage which has been sampled in the sampling step, to generate the second binary code.

3. An A/D conversion method for a serial/parallel A/D converter

which compares an analog input voltage which randomly varies with time and a prescribed first reference voltage, to generate a first binary code, as well as repeatedly compares a reference voltage which is decided on the basis of the result of the comparison and the analog input voltage to generate a binary code, thereby generating second to n-th ("n" is an integer satisfying $n \geqq 3$) binary codes, and performs a logic operation on the generated first to n-th binary codes, thereby generating a digital value, said method comprising steps of:

sampling the analog input voltage received, as well as initializing previous second to n-th reference voltages to a prescribed initialization voltage; and

carrying out an m-th voltage comparison step ("m" is an integer satisfying $1 \leqq m < n$) of comparing the value of the analog input voltage which has been sampled in the sampling and initialization step and the m-th reference voltage, to generate the m-th binary code, and an (m+1)-th voltage comparison step of comparing the value of the (m+1)-th reference voltage which has been changed from the prescribed initialization voltage to a voltage value which is decided on the basis of the result of the comparison in the m-th voltage comparison step and the value of the analog input voltage which has been sampled in the sampling and initialization step, to generate the (m+1)-th binary code, from m=1 to m=n-1.

4. An A/D conversion method for a serial/parallel A/D converter which compares an analog input voltage which randomly varies with time and a prescribed first reference voltage, to generate a first binary code, as well as repeatedly compares a reference voltage which is decided on the basis of the result of the comparison and the analog input voltage to generate a binary code, thereby generating second to n-th ("n" is an integer satisfying $n \geqq 3$) binary codes, and performs a logic operation on the generated first to n-th binary codes, thereby generating a digital value, said method comprising steps of:

sampling the analog input voltage received; and

carrying out an m-th voltage comparison and initialization step ("m" is an integer satisfying $1 \leqq m < n$) of comparing the value of the analog input voltage which has been sampled in the sampling step and the m-th reference voltage, as well as initializing a previous (m+1)-th reference voltage to a prescribed initialization voltage, to generate the m-th binary code, and an (m+1)-th voltage comparison step of comparing the value of the (m+1)-th reference voltage which has been changed from the prescribed initialization voltage to a voltage value which is decided on the basis of the result of the comparison in the m-th voltage comparison and initialization step and the value of the analog input voltage which has been sampled in the sampling step, to generate the (m+1)-th binary code, from m=1 to m=n-1.

5. A serial/parallel A/D converter for converting an analog input voltage into a digital value, comprising:

a reference resistor and switch array which is constituted by a resistor array comprising plural resistors which are serially connected, and plural switches connected to plural connection points of the resistor array, for selectively outputting a reference voltage which is compared with the analog input voltage that randomly varies with time;

a first voltage comparator array for sampling the analog input voltage received, and comparing the sampled analog input voltage and a first reference voltage which is output from the reference resistor and switch array, to output a first comparison result;

a first code selecting circuit which receives the first comparison result output from the first voltage comparator array, and outputs a first code selection signal;

a first coding circuit which outputs a first binary code that is selected in accordance with the first code selection signal output from the first code selecting circuit;

a second voltage comparator array for sampling the analog input voltage received, and comparing the sampled analog input voltage and a second reference voltage which is selectively output by the plural switches constituting the reference resistor and switch array in accordance with the first code selection

signal, to output a second comparison result;

a second code selecting circuit which receives the second comparison result output from the second voltage comparator array, and outputs a second code selection signal;

a second coding circuit which outputs a second binary code which is selected in accordance with the second code selection signal output from the second code selecting circuit; and

a code compositing circuit which performs a logic operation on the first binary code and the second binary code, to obtain a digital value, wherein

said second voltage comparator array samples the received analog input voltage, receives and holds a prescribed initialization voltage in an arbitrary period of time, and compares the value of the second reference voltage which has been changed from the prescribed initialization voltage to a voltage value which is selectively output by the plural switches constituting the reference resistor and switch array in accordance with the first code selection signal, and the value of the sampled analog input voltage.

6. The serial/parallel A/D converter of Claim 5 wherein

the initialization voltage is a reference voltage which is output from one of the plural connection points of the resistor array constituting the reference resistor and switch array.

7. The serial/parallel A/D converter of Claim 5 further including:

a reference voltage initializing circuit which receives the second reference voltage output from the reference resistor and switch array, the initialization voltage, and an initialization control signal indicating the arbitrary period, and outputs either the second reference voltage or the prescribed voltage to the second voltage comparator array in accordance with the initialization control signal, wherein

said reference voltage initializing circuit outputs the initialization voltage in the arbitrary period, while outputting the second reference voltage which is output from the reference resistor and switch array in periods other than the arbitrary period.

8. The serial/parallel A/D converter of Claim 5 wherein

said first code selecting circuit receives an initialization control signal indicating the arbitrary period, as well as the first comparison result output from the first voltage comparator array, and

in the arbitrary period, the first code selection signal is output to the first coding circuit, as well as an initialization voltage selection signal for selecting the prescribed initialization voltage by fixing predetermined switches among the plural switches constituting the reference resistor and switch

array in on-state while fixing all other switches in off-state is output to the reference resistor and switch array, and

in periods other than the arbitrary period, the first code selection signal is output to the first coding circuit and the reference resistor and switch array.

9. The serial/parallel A/D converter of Claim 5 wherein

said arbitrary period is a period during which the analog input voltage input is sampled in the first and second voltage comparator arrays.

10. The serial/parallel A/D converter of Claim 5 wherein

said arbitrary period is a period during which the first voltage comparator array compares the analog voltage value and the first reference voltage which is output from the reference resistor and switch array, and outputs the first comparison result.

11. A serial/parallel A/D converter for converting an analog input voltage into a digital value, comprising:

a reference resistor and switch array which is constituted by a resistor array comprising plural resistors which are serially connected, and plural switches connected to plural connection points of the resistor array, for selectively outputting a reference voltage which is compared with the analog input voltage

that randomly varies with time;

a first voltage comparator array for sampling the analog input voltage received, and comparing the sampled analog input voltage and a first reference voltage which is output from the reference resistor and switch array, to output a first comparison result;

second to n-th voltage comparator arrays for sampling the analog input voltage received, and comparing the sampled analog input voltage and second to n-th reference voltages which are generated in the reference resistor and switch array on the basis of comparison results from the first to (n-1)-th ("n" is an integer satisfying $n \geqq 3$) voltage comparator arrays, respectively, to output second to n-th comparison results, respectively;

first to n-th code selecting circuits which receive the first to n-th comparison results output from the first to n-th voltage comparator arrays, respectively, and output first to n-th code selection signals, respectively;

first to n-th coding circuits which output first to n-th binary codes which are selected in accordance with the first to n-th code selection signals output from the first to n-th code selecting circuits, respectively; and

a code compositing circuit which performs a logic operation on the first to n-th binary codes output from the first to n-th coding circuits, to obtain a digital value, wherein

each of said second to n-th voltage comparator arrays samples

the analog input voltage, receives and holds a prescribed initialization voltage in an arbitrary period of time, and compares each value of the second to n-th reference voltages which has been changed from the prescribed initialization voltage to a voltage value that is selectively output by the plural switches constituting the reference resistor and switch array adaptively to the respective first to (n-1)-th code selection signals, with the value of the sampled analog input voltage.